Please amend the claims as follows:

1(Currently amended). A reconfigurable chip including a reconfigurable functional unit having a modified input multiplexer unit ~~that can select~~ configured to select a combined value, the combined value including some of the bits from an output of the reconfigurable functional unit and at least one bit from another reconfigurable functional unit.

2(Original). The reconfigurable chip of Claim 1 wherein at least one bit from another reconfigurable functional unit is the carry bit from another reconfigurable functional unit.

3(Currently amended). The reconfigurable chip of Claim 1 wherein ~~the shifted version of~~ said some of the bits comprise all but the most significant bit of the output of the reconfigurable functional unit shifted left one space.

4(Original). The reconfigurable chip of Claim 1 wherein the reconfigurable functional unit and another reconfigurable functional unit implements a linear feedback shift register.

5(Original). The reconfigurable chip of Claim 1 wherein the modified input multiplexer unit includes circuitry to switch between a combined value and other values.

6(Currently amended). The ~~modified input multiplexer unit~~ reconfigurable chip of Claim 1 wherein conductive lines on the reconfigurable chip arrange the combined value as an input to a multiplexer in the modified multiplexer unit.

7(Original). The reconfigurable chip of Claim 1 wherein the combined value includes all but one bit of the output of the reconfigurable functional unit and the carry bit from another reconfigurable functional unit wherein if the most significant

PAGE 8/12 * RCVD AT 5/26/2005 6:58:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):03-32

bit of the output of the reconfigurable functional unit is in a predetermined state, the reconfigurable functional unit is configured to provide a mask value from a register and the reconfigurable functional unit is configured to exclusive OR the combined value to a mask value to produce a new output value.

8(Currently amended). An implementation of a linear feedback shift register on a reconfigurable chip wherein a first reconfigurable functional unit is adapted to provide at least one input bit to a second reconfigurable functional unit, the second reconfigurable functional unit having a modified input multiplexer unit ~~that can select~~ configured to select a combined value, the combined value including some of the bits from an output of the second reconfigurable functional unit and the at least one input bit from the first reconfigurable functional unit.

9(Currently amended). The implementation of Claim 8 wherein the at least one input bit is a carry bit from the first reconfigurable functional unit.

10(Original). The implementation of Claim 9 wherein the first reconfigurable functional unit is adapted to add an input value to itself so that the carry bit contains a most significant bit of the input value.

11(Original). The implementation of Claim 8 wherein if the most significant bit of the output of the second reconfigurable functional unit is in a predetermined state, the second reconfigurable functional unit is configured to provide a mask value from a register and a second reconfigurable functional unit is configured to Exclusive-OR the combined value to the mask value to provide a new output value.

12(Original). The implementation of Claim 8 wherein the modified input multiplexer unit includes lines to provide an input of the combined value to a multiplexer in a modified input multiplexer unit.

PAGE 9/12 * RCVD AT 5/26/2005 6:58:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):03-32

13(Original). The implementation of Claim 8 wherein the modified input multiplexer unit allows the selection between the combined value and the output of the second reconfigurable functional unit.

14(Original). An implementation of a linear feedback shift register on a reconfigurable chip wherein a first reconfigurable functional unit is configured to add an input value to itself so that a carry bit contains the most significant bit of the input value, the second reconfigurable functional unit having a modified input multiplexer unit configured to select a combined value, the combined value including all but one bit of the output of the second reconfigurable functional unit and the carry bit from the first reconfigurable functional unit, wherein if the most significant bit of the output of the second reconfigurable functional unit is configured to provide a mask value from a register and the second reconfigurable functional unit is configured to exclusive-OR the combined value to the mask value to produce an new output value.

15(Original). The implementation of Claim 14 wherein the modified input multiplexer unit includes conductive lines to provide the combined value as an input to a multiplexer in the modified input multiplexer unit.

16(Original). The implementation of Claim 14 wherein the modified input multiplexer unit allows the selection between the output of the second reconfigurable functional unit and the combined value.

17(Original). The implementation of Claim 14 wherein the predetermined state is a one.

18(Original). The implementation of Claim 14 wherein the mask value implements the taps on the linear feedback shift register.

PAGE 10/12 * RCVD AT 5/26/2005 6:58:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):03-32

19(Original). The implementation of Claim 14 wherein the mask value is ANDed together with a value that is all ones if the most significant bit of the output of the reconfigurable functional unit is a one or it's all zeros if the most significant bit of the output of the reconfigurable functional unit is a zero.

20(Original). The method of Claim 19 wherein the output of the second reconfigurable functional unit is sent to a shift register with sign extension such that the output of the shift register is the same in all bits as the most significant bit of the output of the reconfigurable functional unit.

21(Currently amended). The implementation of Claim 14 wherein the sum of the input value and itself is used as a new input value to the first reconfigurable functional unit.

PAGE 11/12 * RCVD AT 5/26/2005 6:58:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):03-32